Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended): A precise slew rate control line driver comprising:

a slew rate control circuit for controlling [[the]] slew rate comprising:

a first operational amplifier comprising a positive input end, a negative input end, and an output end; and

a second operational amplifier comprising a positive input end connected to the positive input end of the first operational amplifier, a negative input end connected to the negative input end of the first operational amplifier, and an output end;

a first driver for driving output signals comprising:

a first current source comprising a first end connected to a voltage source, a second end connected to the positive input end of the first operational amplifier, and a control end connected to the output end of the first operational amplifier or the voltage [[end]] source via a first group of switches; and

a second current source comprising a first end connected to the positive input end of the second operational amplifier, a second end connected to a ground end, and a control end connected to the output end of the second operational amplifier or the ground end via a second group of switches; and

a second driver for setting up transient slope comprising:

a capacitor comprising a first end connected to the negative end of the first operational amplifier, and a second end connected to the ground end;

a third current source comprising a first end connected to the voltage source, a second source connected to the first end of the capacitor, and a control end connected to a first bias signal source or the voltage source via a third group of

switches; and

a fourth current source comprising a first end connected to the first end of the capacitor, a second source connected to the ground end, and a control end connected to a second bias signal source or the ground end via a fourth group of switches.

Claim 2 (Original): The line driver of claim 1 wherein the first current source and the third current source are PMOS transistors with a drain as the first end, a source as the second end, and a gate as the control end.

Claim 3 (Original): The line driver of claim 1 wherein the second current source and the fourth current source are NMOS transistors with a drain as the first end, a source as the second end, and a gate as the control end.

Claim 4 (Original): The line driver of claim 1 wherein the first group of switches comprises two switches for switching the control end of the first current source to be connected to the voltage source or the output end of the first operational amplifier.

Claim 5 (Original): The line driver of claim 1 wherein the second group of switches comprises two switches for switching the control end of the second current source to be connected to the ground end or the output end of the second operational amplifier.

Claim 6 (Original): The line driver of claim 1 wherein the third group of switches comprises two switches for switching the control end of the third current source to be connected to the voltage source or the first bias signal source.

Claim 7 (Original): The line driver of claim 1 wherein the fourth group of switches comprises two switches for switching the control end of the fourth current source to

be connected to the ground end or the second bias signal source.

Claim 8 (Original): The line driver of claim 1 further comprising a first capacitor and a first resistor connected serially between the positive input end and the output end of the first operational amplifier.

Claim 9 (Original): The line driver of claim 1 further comprising a second capacitor and a second resistor connected serially between the positive input end and the output end of the second operational amplifier.

Claim 10 (Original): The line driver of claim 1 wherein the first operational amplifier and the second operational amplifier are inputs rail-to-rail operational amplifiers.

Claim 11 (Currently Amended): A method for controlling the line driver said in claim 1, said method comprising:

(a) switching the first group of switches within the line driver to connect the control end of the first current source with the output end of the first operational amplifier;

switching the second group of switches within the line driver to connect the control end of the second current source with the ground end;

switching the third group of switches within the line driver to connect the control end of the third current source with the first bias signal source; and

switching the fourth group of switches within the line driver to connect the control end of the fourth current source with the ground end; and

(b) switching the first group of switches within the line driver to connect the control end of the first current source with the voltage source;

switching the second group of switches within the line driver to connect the control end of the second current source with the output end of the second

operational amplifier;

switching the third group of switches within the line driver to connect the control end of the third current source with the voltage source; and

switching the fourth group of switches within the line driver to connect the control end of the fourth current source with the second bias signal source.

Claim 12 (Currently Amended): The method of claim 11 wherein ~~Step(a)~~ steps (a) and (b) are ~~executed~~ performed in different periods of time.